WHAT IS CLAIMED IS

1. A method for partitioning allocation and management of jitter buffer memory for TDM circuit emulation applications comprising the steps of:

a. obtaining a channel hierarchy for a plurality of packet carrying channels having different channel rates;

b. obtaining for each packet a respective packet sequential number; and

c. generating a segment base-address in the jitter buffer memory using said channel hierarchy and said respective packet sequential number;

whereby said partitioning allocation and management of the jitter buffer memory is correlated with said generated segment base-address such that each said channel is allocated a space in a buffer memory of a given size, said space being proportional to a respective said channel rate, and whereby out-of-order packets are automatically reordered by the jitter buffer.

2. The method of claim 1, wherein said step of obtaining a channel hierarchy includes obtaining a channel hierarchy for at least two of channels of said plurality that include packets of different size.

3. The method of claim 2, wherein said step of obtaining a channel hierarchy further includes obtaining a channel identification (CH-ID) number.

4. The method of claim 3, wherein said obtaining of a CH-ID number includes obtaining a CH-ID number of 9 bits.

5. The method of claim 4, wherein each said packet includes a CEP header, and wherein said step of obtaining a packet sequential number includes obtaining a 14 bit sequential number from said CEP header.

6. The method of claim 3, wherein said generating a segment base-address in the jitter buffer memory includes dividing said jitter buffer memory into a plurality of hierarchically

arranged queues and allocating each said queue to one said channel, so that the queue hierarchy follows said channel hierarchy

7. The method of claim 6, wherein said step of generating a segment base-address includes determining an address size based on said jitter buffer memory size.

8. The method of claim 7, wherein said determining an address size based on said jitter buffer memory size further includes:

i. determining a number of address bits as a log2 of said jitter buffer memory size,

ii. determining a number M of upper bits for a respective channel using said CH-ID number

ii. determining a byte-offset size that includes a number N of lowermost bits allocated for a byte offset,

iv. determining a number P of remaining bits from said packet sequential number,

v. selecting a number of effective channel identification bits from said CH-ID, and

vi. selecting an effective part of said packet sequential number.

9. The method of claim 6, wherein said dividing said jitter buffer memory into a plurality of hierarchically arranged queues includes partitioning said jitter buffer memory into said queues by using powers of 2 division factors.

10. A hierarchically partitioned jitter buffer memory comprising:

a. a plurality of hierarchically arranged queues correlated with a channel hierarchy; and

b. a mechanism for addressing said hierarchically arranged queues.

11. The jitter buffer memory of claim 10, wherein said hierarchically arranged queues are further divided into segments, each said segment designed to hold one packet.

12. The jitter buffer memory of claim 11, wherein each of said segments is characterized by a size in bytes correlated with a maximum packet size carried by a respective said channel.

13. The jitter buffer memory of claim 11, wherein the number of said segments in bytes is an integer power of 2.

14. The jitter buffer memory of claim 13, wherein said segment size is the minimum integer power of 2 that can hold said maximum packet size.

15. A method for partitioning allocation and management of jitter buffer memory for TDM circuit emulation applications comprising the steps of:

a. obtaining a channel hierarchy for a plurality of packet carrying channels having different channel rates;

b. dividing the jitter buffer memory into a plurality of hierarchically arranged queues; and

c. allocating each said hierarchically arranged queue to a respective said channel so that said queue hierarchy follows said channel hierarchy;

whereby the jitter buffer memory can be advantageously optimized for TDM emulation by a hierarchical partitioning that follows the SONET/SDH hierarchy.

16. The method of claim 15, wherein said step of obtaining a channel hierarchy includes obtaining a channel hierarchy for at least two of channels of said plurality that include packets of different size.

17. The method of claim 16, wherein said step of obtaining a channel hierarchy further includes obtaining a channel identification (CH-ID) number.

18. The method of claim 17, wherein said obtaining of a CH-ID number includes obtaining a CH-ID number of 9 bits.

19. The method of claim 15, wherein said dividing the jitter buffer memory into a plurality of hierarchically arranged queues includes partitioning said jitter buffer memory into said queues by using powers of 2 division factors.